REMARKS

Claims 1, 2, 4-17, 31, and 33 remain pending in this application for which applicants seek reconsideration. Claim 3 has been canceled, and claim 1 has been amended to include the subject matter of canceled claim 3 and to clarify that the first and second semiconductor regions are alternately arranged along the loop. Claim 4 has been amended to depend from claim 1. Claims 6, 8, 9, 11, 12, and 14 also have been amended to remove minor informalities contained therein. Specifically, the antecedent basis problem in claim 6 has been obviated by changing "the" to --a-- in both instances. These claims also have been further amended to remove a minor antecedent basis problem regarding "sections." Note that a singular "section" is more appropriate since claim 6 recites at least one rather than a plurality. No new matter has been introduced.

Allowable Claims

Claim 2 has been allowed, and claims 6 and 7 were indicated to be allowable if the antecedent basis problem is overcome. Applicants note that claims 8-12 also properly depend from claim 6, which is believed to be generic to these claims. Accordingly, these claims should be also allowed with claims 6 and 7 (in contrast to the assertion made in paragraph 1 of the Detailed Action that there is no allowable generic claim).

Art Rejection

Claims 1, 3, 4, 14, and 31 were rejected under 35 U.S.C. § 103(a) as unpatentable over Coe (USP 4,754,310) in view of Fujihira (USP 6.097,063). Applicants traverse this rejection to the extent that these references do not teach first and second semiconductor regions arranged alternately along the direction of the loop as now called for in claim 1.

Coe, in contrast, teaches a loop, but the first and second semiconductor regions are not alternately arranged along the direction of the loop, but rather perpendicular to it. That is, Coe's first and second semiconductor regions do not alternate along the same plane but are rather vertically stacked, as acknowledged by the examiner. In this regard, the examiner relies on Fujihira for the proposition that it would have been obvious to alternately arrange the first and

second semiconductor regions along the surface. Applicants disagree. The combination would not have taught alternately arranged first and second semiconductor regions forming a curved section because neither of the applied references teaches a curved section.

Moreover, applicants submit that there would not have been any motivation for one of ordinary skill in the art to arrange the first and second semiconductor regions to surround an electrode in the manner claimed. Note that the examiner's assertion that Fujihira's arrangement would decrease the ON-resistance is untenable since Coe's structure is entirely different, and Fujihira merely discloses that ON-resistance can be reduced in comparison to a conventional device. There is no teaching anywhere that Fujihira's configuration would be beneficial or superior over Coe's configuration.

Conclusion

Applicants submit that the applied references do not teach the claimed loop configuration formed by alternately arranged first and second semiconductor regions. Applicants therefore urge the examiner to enter the present Amendment and issue an early Notice of Allowance. Should the examiner have any issues concerning this reply or any other outstanding issues remaining in this application, applicants urge the examiner to contact the undersigned to expedite prosecution.

Respectfully submitted,

Date: 12/04/02

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ATTACHMENT

MARKED UP VERSION

IN THE CLAIMS:

Claims 1, 4, 6, 8, 9, 11, 12, and 14 have been amended as follows:

--1. (Twice Amended) A lateral semiconductor device comprising:

a semiconductor chip;

two main electrodes on one major surface of the semiconductor chip; and

an alternating conductivity type layer between the main electrodes;

wherein the alternating conductivity type layer comprises first semiconductor regions of a first conductivity type and second semiconductor regions of a second conductivity type;

wherein the first semiconductor regions and the second semiconductor regions are alternately arranged in a surface portion of the major surface; [and]

wherein the alternating conductivity type layer comprises a closed loop formed by the first and second semiconductor regions alternately arranged along the direction of the closed loop and surrounding one of the main electrodes; and

wherein the alternating conductivity type layer comprises at least one straight section and at least one curved section.--

--4. (Amended) The lateral semiconductor device according to Claim [3]1, wherein the alternating conductivity type layer comprises at least two straight sections and at least two curved sections.--

--6. (Twice Amended) A lateral semiconductor device comprising:

a semiconductor chip;

two main electrodes on one major surface of the semiconductor chip; and

an alternating conductivity type layer between the main electrodes;

wherein the alternating conductivity type layer comprises first semiconductor regions of a first conductivity type and second semiconductor regions of a second conductivity type;

wherein the first semiconductor regions and the second semiconductor regions are

alternately arranged;

wherein the alternating conductivity type layer comprises a closed loop surrounding one of the main electrodes;

wherein the alternating conductivity type layer comprises at least one straight section and at least one curved section; and

wherein the first semiconductor regions and the second semiconductor regions are arranged alternately at [the] a first pitch in the straight section[s], and the first semiconductor regions and the second semiconductor regions are arranged alternately at [the] a second pitch in the curved section[s].--

--8. (Amended) The lateral semiconductor device according to Claim 6, wherein the curved section[s are] is doped substantially more lightly than the straight section[s].

9. (Amended) The lateral semiconductor device according to Claim 8, wherein the curved section[s are] is substantially intrinsic.--

--11. (Amended) The lateral semiconductor device according to Claim 8, wherein the curved section[s are] is doped with an n-type impurity and a p-type impurity.

12. (Amended) The lateral semiconductor device according to Claim 9, wherein the curved section[s are] is doped with an n-type impurity and a p-type impurity.--

--14. (Amended) The lateral semiconductor device according to Claim 1, further comprising [one or more] a plurality of closed loops, each including [an] the alternating conductivity type layer.--